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Application Note

24B752XA

Wide VGA B&W CMOS Board Camera

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Doc # APN 24B752xA	Issue Date: 11/21/2008
Revision: C	Page 1 of 22

Table Of Contents

1.	Introduction	3
2.	History.....	3
3.	Applications.....	3
4.	Features	3
5.	Block Diagram	4
6.	Video Outputs.....	4
7.	Digital Output Modes	5
8.	Window Control (Digital and LVDS output only)	6
9.	Area of Interest Selection:	7
10.	Frame Rate	7
11.	Pixel Integration Control	8
12.	Gain Settings.....	9
12.1.	Automatic Gain Control (AGC) and Automatic Exposure Control (AEC).....	10
13.	Table of Registers	12
14.	Mechanical Dimensions	20
15.	Connection Diagram	21
16.	Contact	22

1. Introduction

The 2xB752x is a 1/3" B&W CMOS camera based on the Micron MT9V022 WVGA sensor. It's small board design (29 x 29 mm) along with its wide temperature and vibration specification allows it to be used in automotive to security applications now and far into the future.

2. History

Revision	Issue Date	Reason	CN#
Rev A	09-19-2007	Initial release	07-0217
Rev B	10-30-2007	Added connector diagram (section 15)	07-0245
Rev C	11-10-2008	Dimensions corrected	08-0187

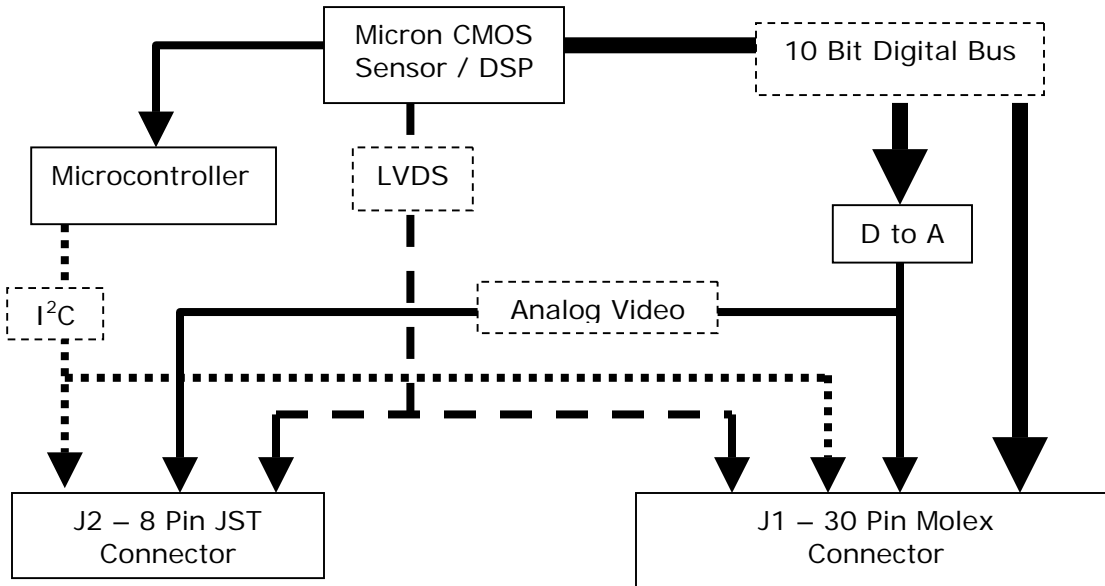
3. Applications

- Automotive
- Security / surveillance
- Automation
- Machine vision

4. Features

- Micron MT9V022 1/3" WVGA CMOS sensor
- CVBS / LVDS or Digital output
- Near IR performance
- Interlaced (analog / digital) & progressive (digital) output modes
- Linear or high dynamic range
- Global shutter
- I2C control
- Wide operating temperature range from -40 to 80° C
- 2x2 & 4x4 binning to improve sensitivity in smaller resolutions
- Windowing
- Column and row mirroring
- Parallel low voltage, transistor – transistor logic (LVTTTL output)

5. Block Diagram



6. Video Outputs

CVBS – With a 13.5Mhz crystal in position X2 the CVBS output (pin 3 of J2 and Pin 29 of J1) is standard NTSC format.

LVDS – The LVDS output is enabled at pin 14 &16 of connector J1 and Pin 7 & 8 of connector J2 with a 26.6Mhz crystal in position X2, bit 4 of address 0xB3 changed to 0 and bit 1 of address 0xB1 changed to 0.

The LVDS interface allows for the streaming of sensor data serially to a standard off the shelf de-serializer up to 5 meters away from the sensor. The serial link can save on cabling cost of 14 wires (Dout 0-9, Line_valid, Frame_Valid, Pixel CLK, and ground) instead, just 3 wires (2 Differential & 1 ground) are sufficient to carry the video signal.

The packet size is 12 bits (2 frame bits and 10 payload bits) and 10-bit pixel or 8-bit pixel format can be selected. In 8-bit pixel mode, the packet consists of a start bit, 8 bit pixel data (w/ sync codes), the line valid bit, the frame valid bit and the end bit.

For the 10-bit pixel mode, the packet consists of a start bit, 10 bit pixel data, and the end bit.

12 bit packet	8 bit pixel mode	10 bit pixel mode
Bit (0)	Start Bit	Start Bit
Bit (1)	Pixel Data (2)	Pixel Data (0)
Bit (2)	Pixel Data (3)	Pixel Data (1)
Bit (3)	Pixel Data (4)	Pixel Data (2)
Bit (4)	Pixel Data (5)	Pixel Data (3)
Bit (5)	Pixel Data (6)	Pixel Data (4)
Bit (6)	Pixel Data (7)	Pixel Data (5)
Bit (7)	Pixel Data (8)	Pixel Data (6)
Bit (8)	Pixel Data (9)	Pixel Data (7)
Bit (9)	Line_Valid	Pixel Data (8)
Bit (10)	Frame_Valid	Pixel Data (9)
Bit (11)	Stop Bit	Stop Bit

7. Digital Output Modes

Interlaced: The camera has two interlaced readout options. By setting register 0x07 bits 0-2 to 1 all the even numbered rows are read out first, followed by a number of programmable field blank (register 0x08 bits 0-7), then the odd numbered rows and finally vertical blank (minimum is 4 blank rows).

By setting register 0x07 bits 0-2 to 2 only one field is read out consequently, the number of rows read out is half what is set in register 0x03. The two start address (register 0x02) determines which field gets read out: if row start address is even an even field is read out, if row start address is odd an odd field is read out.

Similar to progressive scan, frame valid is logic low during valid image row only.

Field blanking = Register 0xBF bits 0-7

Vertical Blanking = Register -x06 bits 0-8 minus register 0xBF bits 0-7

With minimum vertical blank requirement = 4.

Progressive: The camera can also be read out in a progressive scan mode. Horizontal and vertical blanking surrounds valid image data. The amount of horizontal and vertical blanking is programmable through registers 0x05 and 0x06 respectively.

The data output is synchronized with the pixel clock output. When "Line Valid" is high, one 10-bit pixel packet is output for every pixel clock period. The pixel clock is the nominally inverted version of the master clock (SYSCLK).

This allows the pixel clock to be used as a clock to latch the data; however, when the column bit 2 is enabled the pixel clock is high for one complete master clock period and low for one complete master clock period. When the column bit 4 is enabled the pixel clock is high for 2 complete master clock periods. It is continuously enabled, even during the blanking period.

Setting register 0x74 bit 4 to 1 causes the camera to invert the polarity of the pixel clock. The recommended master clock frequency is 26.6Mhz for the digital and LVDS outputs.

Doc # APN 24B752xA	Issue Date: 11/21/2008
Revision: C	Page 5 of 22

8. Window Control (Digital and LVDS output only)

Registers 0x01 (column start), 0x02 (row start), 0x03 (window height) and 0x04 (window width) control the size and coordinates of the window.

The values programmed in the window height and width registers are the exact window height and width out of the camera's sensor. The window start value should never be set below 4. To read out the dark rows set register 0x0D bit 6. In addition bit 7 can be used to display the dark columns in the image.

Pixel Binning: In addition to the windowing mode, where smaller resolution (CIF, QCIF) is obtained by selecting small window from the sensor array, the camera also provides the ability to show the entire image captured by pixel array with smaller resolution by pixel binning.

Pixel binning is based on combining signals from adjacent pixels by averaging. There are two options, binning 2 and binning 4. Binning 2 is 4 pixels that are combined from 2 adjacent rows and columns. The binning 4 mode is 16 pixels that are combined from 4 adjacent rows and columns.

The image mode may work in conjunction with image flip. The binning operation increases the signal to noise ratio (SNR) but decreases the resolution.

Row Bin: By setting bit 0 or 2 of register 0x0d only $\frac{1}{2}$ or $\frac{1}{4}$ of what is set in register 0x03 is read out.

Column Bin: By setting bit 1 or 3 of register 0x0D the pixel data rate is slowed down by a factor of either 2 or 4 respectively. This is due to the overhead time in the digital pixel data processing chain. As a result, the clock speed is also reduced accordingly.

Column Flip: By setting bit 5 of register 0x0D the readout order of the columns is reversed.

Row Flip: By setting bit 4 of register 0x0D the readout order of the rows is reversed.

9. Area of Interest Selection:

To access an area of interest on this camera you must change several registers in order to define the starting column and row along with the height and width of the image to be read out.

1. Select the column in which to start by entering the column number at register 01 in 2 byte Hex format. You have a choice of 1-752 (0001-02F0 Hex) columns that are optically active.
2. Select the row in which to start by entering the row number at register 02 in 2 byte Hex format. You have a choice of 4-482 (0004-01E2 Hex) rows. Setting a value of less than four is not recommended.
3. Select the window height by entering the number of rows in the image to be read out at register 03 in 2 byte hex format. You have a choice of 1-480 (0001-01E0 Hex) that may be read.
4. Select the window width by entering the number of columns in the image to be read out at register 04 in 2 bit hex format. You have a choice of 1-752 (0001-02F0) that may be read.

For example: To select an area of interest in the center of the screen that is 10 columns high and 10 rows wide you would enter the following – In register 02 (column start) you would put the data 0173.

In register 03 (Row start) you would put the data 00EA.

In register 04 (Window height) you would put the data 000A. And in register 05 (Window width) you would put the data 000A.

10. Frame Rate

The standard frame of this camera is 60 fps at full resolution but by changing register 0x0D bits 0-1 to 10 (row bin 2) or 01 (row bin 4) you can enable row binning of 2 rows or 4 rows.

With this you can increase the frame rate by 2 and 4 respectively. This increase does however reduce the size of the image by $\frac{1}{2}$ and $\frac{1}{4}$ respectively.

*****Note: Binning and area of interest should not be used in conjunction with the interlaced mode.*****

Doc # APN 24B752xA	Issue Date: 11/21/2008
Revision: C	Page 7 of 22

11. Pixel Integration Control

Total integration: Register 0x0B (total shutter width) along with the window width and horizontal blanking registers, control the integration time for the pixels. The actual total integration time is the number of rows of integration multiplied by the row time, where the number of rows of integration is equal to the result of automatic exposure control (AEC).

This may vary from frame to frame or if (AEC) is disabled, the value in register 0x0B, row time equals register 0x04 + register 0x05 master clock periods. Typically the value of register 0x0B (total shutter width) is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time.

If register 0x0b is increased beyond the total number of rows per frame, it is required to add additional blanking rows using register 0x06 as needed.

A second constraint is that the total integration time must be adjusted to avoid banding in the image from light flicker under 60hz.

Flicker means the frame time must be a multiple of 1/120 second and under 50hz flicker the frame time must be a multiple of 1/100 second.

High Dynamic Range: By adjusting the following registers: 0x08 (shutter width), 0x09 (shutter width 2), and 0x31-34 (V_step voltages) high dynamic range (HDR) is achieved by controlling the saturation level of the pixel during the exposure period.

After the pixels are reset, the step voltages, V_step, which is applied to the HDR gate, is setup at V1 for integration time T1 then to V2 for time T2, then V3 for time T3, and finally it is parked at V4, which also serves as an anti-blooming voltage for the photo detector.

This sequence of voltages leads to a piece-wise linear pixel response. The parameters of the voltage V_step take values V1, V2 & V3 and directly effect the position of the knee points.

Light intensities work approximately as a reciprocal of the partial exposure time. Typically T1 is the largest exposure T2 shorter and so on. Thus the ranges of light intensities are shortest for the first slope, providing the highest sensitivity.

Register settings for V_step and partial exposures:

V1 = register 0x31 bits 0-4

V2 = register 0x32 bits 0-4

V3 = register 0x33 bits 0-4

V4 = register 0x34 bits 0-4

Total integration time = T1 + T2 + T3

There are two ways to specify the knee point timing; the first is by manually setting and the second by automatic knee point adjustment. When the auto adjust is set to high the camera calculates the knee points automatically using the following equations:

T1 = Total Integration time – T2 – T3

T2 = Total Integration time * ½ (register 0x0A bits 0-3)

T3 = Total Integration time * ½ (register 0x0A bits 4-7)

For auto exposure T2 = 1/16th of the total integration time and T3 is 1/64th of the total integration time. When the auto adjust is disabled T1, T2 and T3 may be programmed via I2C:

Doc # APN 24B752xA	Issue Date: 11/21/2008
Revision: C	Page 8 of 22

T1 = register 0x08 bits 0-14

T2 = (register 0x09 bits 0-4) – (register 0x08 bits 0-14)

T3 = Total Integration time – T1 – T2

The total integration time may be based on the manual setting of register 0x0b or the result of AEC. If the AEC is enabled then the auto knee adjust must also be enabled. Register 0x0A bit 9 should equal 1 for auto enable.

Variable ADC Resolution:

By Default, ADC resolution of the sensor is 10 bit. Additionally, a companding scheme of 12-bit into 10-bit is enabled by changing register 0x1C bit 0 to a 1 for 12 to 10 companding and a 0 for 10-bit linear.

This mode allows higher ADC resolution which means less quantization noise at low light and lower resolution at higher light levels where good ADC quantization is not so critical because of the high level of the photon shot noise.

12. Gain Settings

Changes to gain settings:

When the digital gain settings (register 0x80 – 98) are changed, the gain is updated on the next frame start. However, the latency for an analog gain change to take effect depends on the automatic gain control.

If automatic gain control is enabled (register 0xAF bit 1 set to 1) the gain changed for frame (n) first appears in frame (n+1); if the automatic gain control is disabled, the gain changed for frame (n) first appears in frame (n+2). Both analog and digital gain changes regardless of whether the integration time is also changed simultaneously.

Analog Gain: (Register 0x35 global gain)

Formula for gain setting: Gain = (bits 0-6) * (0.0625)

The analog gain range supported in the camera is 1x –4x with a step size of 6.25%. In order to manually control gain with this register, the camera must not be in AGC mode. When adjusting the luminosity of an image it is recommended to alter the exposure first and yield to gain increased only when the exposure value has reached a maximum limit.

Digital Gain: Register 0x80-98 Tiled Digital Gain & weight. Registers 0x99-A4 Tile coordinates.

In the camera the image may be divided into 25 tiles using I2C and apply digital gain individually to each tile. Registers 0x99-9E represent X1-5 and registers 0x9F – A4 represent Y1 – 5.

Doc # APN 24B752xA	Issue Date: 11/21/2008
Revision: C	Page 9 of 22

	X0	X1	X2	X3	X4	X5
Y0	X0/Y0	X1/Y0	X2/Y0	X3/Y0	X4/Y0	
Y1	X0/Y1	X1/Y1	X2/Y1	X3/Y1	X4/Y1	
Y2	X0/Y2	X2/Y2	X2/Y2	X3/Y2	X4/Y2	
Y3	X0/Y3	X1/Y3	X2/Y3	X3/Y3	X4/Y3	
Y4	X0/Y4	X1/Y4	X2/Y4	X3/Y4	X4/Y4	
Y5						

Digital gains of registers 0x80 –98 applies to their corresponding tiles. The camera supports a digital gain of 0.25 to 3.75 X. The formula for digital gain settings is: Digital gain = registers 0x80 – 98 bits 0-3 * 0.25.

12.1. Automatic Gain Control (AGC) and Automatic Exposure Control (AEC)

The integrated AEC/AGC unit is responsible for ensuring that optimal auto setting of exposure and (analog) gain are computed and updated every frame.

AEC & AGC can be individually enabled or disabled by register 0xAF bits 0-1.

When AGC is disabled bit 1 = 0 the sensor uses the manual gain value in register 0x35.

When AEC is enabled bit 1 = 1.

The maximum auto gain value is limited by register 0x36 and the minimum auto gain is fixed at 16 gain units. The exposure control measures current scene luminosity and desired output luminosity by accumulating a histogram of pixel values while reading out a frame. The desired exposure and gain are the calculated from the subsequent frame.

When both AEC and AGC are enabled, only the AEC is initially active with the AGC set at unity gain. The AGC becomes active only when AEC hits maximum row time, causing the AEC to remain at its maximum row time while the gain is increased.

Each histogram bin accumulates 16 pixel intensities. Bin 1 is a collection of all pixel intensities from 0 – 15. Bin 2 is a collection of pixel intensities from 16 to 31 and so on. Since the auto exposure and auto gain controls are histogram based the bin numbers represents a saturation percentile.

The total count of the pixels in the percentile is user definable through register 0xB0 bits 0-15. The user conveys the desired luminosity of the image by setting a desired bin via register 0xA5 bits 0-5. The value can be between 1 and 64.

The current luminosity of the image is available in register 0xBC. It ranges from 1 – 64 and is termed the current bin. For a given image frame, when the total of all pixels in bin 64 + bin 63 ...+ bin (n) is equal to or greater than the saturation percentile (pixel-count value in register 0xB0), then bin (n) is the value of the current bin.

In order to maximize the auto exposure / auto gain response and minimize the settling time (oscillation dying down), the user may need to adjust the low pass filter (LPF) and skip frames values.

The register table describes these controls in register 0xA6, 0xA8, 0xA9 and 0xAB. An LPF value of 0 indicates that the next update will be the newly computed exposure or gain value.

An LPF value of 1 indicates that the next update will be the newly computed exposure or gain value only if the ration of the difference of the calculated value to the current value is more than $\frac{1}{4}$.

If not, only $\frac{1}{2}$ the total change is affected. An LPF value of 2 indicates that the next update will be the newly computed exposure or gain value only if the ration of the difference of the calculated value to the current value is more than $\frac{1}{4}$. If not, only $\frac{1}{4}$ the total change is affected.

The skip frame value conveys how many frames to skip before an updating of the exposure or gain. If the skip frame value is equal to 0, it implies skip 0 frames before update. If the skip frame value is equal to 1, it implies skip 1 frame before update. The maximum skip frame value is 15.

Doc # APN 24B752xA	Issue Date: 11/21/2008
Revision: C	Page 11 of 22

13. Table of Registers

(All registers 16 bit – bits not listed should not be changed)

Register (hex)		Register Name	
Bit	Bit Name	Bit Description	Read/Write
0x00/0xFF		Chip Version	
0-15	Chip version	Chip Version	R
0x01		Column Start	
0-9	Column Start	The first column to be read out (not counting dark columns that may be read). To window the image down, set this register to the starting X value. Readable/active columns are 1-752	W
0x02		Row Start	
0-8	Row Start	The first row to be read out (not counting any dark rows that may be read). To window the image down, set this register to the starting Y value. Setting a value less than four is not recommended since the dark rows should be read using Register 0x0D	W
0x03		Window Height	
0-8	Window Height	Number of rows in the image to be read out (not counting any dark rows or border rows that may be read).	W
0x04		Window Width	
0-9	Window Width	Number of columns in image to be read out (not counting any dark columns or border columns that may be read).	W
0x05		Horizontal Blanking	
0-9	Horizontal Blanking	Number of blank columns in a row. Minimum horizontal blanking is 43 columns.	W
0x06		Vertical Blanking	
0-14	Vertical Blanking	Number of blank rows in a frame. This number must be equal to or larger than four if read dark row control bit (bit 8 of register 0x0d) is set, or two otherwise.	W
0x07		Chip Control	
0-2	Scan Mode	0 = Progressive scan. 1 = not valid 2 = Two-field interlaced scan. Even numbered rows are read first and followed by odd numbered rows. 3 = Single field interlaced scan. If start address is even number, only even numbered rows are read out; if start address is odd number, only odd numbered rows are read out. Effective image size is decreased by half.	W
7	Parallel Output Enable	0 = Disable parallel output. Outputs are High Z 1 = Enable parallel output.	W
8	Simultaneous / Sequential Mode	0 = Sequential mode. Pixel and column readout takes place only after exposure is complete. 1 = Simultaneous mode. Pixel and column readout takes place in conjunction with exposure.	W
9	Defect Pixel Correction Enable	0 = Disable defect pixel correction feature 1 = Enable defect pixel correction feature	W
0x08		Shutter Width 1	
0-14	Shutter Width 1	The row number in which the first knee occurs. This may be used only when high dynamic range option (bit 6 of Register 0x0F) is enabled and exposure knee point auto	W

		<i>adjust control bit is disabled. This register is not showed, but any change made does not take effect until the following new frame.</i>	
0x09		Shutter Width 2	
0-14	Shutter Width 2	<i>The row number in which the second knee occurs. This may be used only when high dynamic range option (bit 6 of register 0x0F) is enabled and exposure knee point auto adjust control bit is disabled. This register is not shadowed, but any change made does not take effect until the following new frame. Shutter width 2 = (bits 14:0) Note: t1 = shutter width 1; t2 = shutter width 2 – shutter 1; t3 = total integration – shutter width 2.</i>	W
0x0A		Shutter Width Control	
0-3	T2 Ratio	<i>One half to the power of this value indicates the ration of duration time t2, when saturation control gate is adjusted to level v2 to total integration when exposure knee point auto adjust control bit is enabled. Any change does not take effect until the following new frame. t2 = Total integration x (1/2)^t2_ratio</i>	W
4-7	T3 Ratio	<i>One half to the power of this value indicates the ratio of duration time t3, when saturation control gate is adjusted to level V3 to total integration when exposure knee point auto adjust control bit is enabled. Any change made does not take effect until the following new frame. t3 = Total integration x (1/2)^t3_ratio. Note: t1 = Total integration – t2 – t3.</i>	W
8	Exposure Knee Point Auto Adjust Enable	<i>0 = Auto adjust disabled. 1 = Auto adjust enabled.</i>	W
9	Single Knee Enable	<i>0 = Single knee disabled. 1 = Single knee enabled.</i>	W
0x0B		Total Shutter Width	
0-14	Total Shutter Width	<i>Total integration time in number of rows. This value is used only when AEC is disabled only (bit 0 of register 0xAF). Any change made does not take effect until the following new frame.</i>	W
0x0C		Reset	
0	Soft Reset	<i>Setting this bit causes the sensor to abandon the current frame by resetting all digital logic except two-wire serial interface configuration. This is a self-resetting register bit and should always read "0". (This bit de-asserts internal active Low reset signal for 15 clock cycles.)</i>	W
1	Auto Block Soft Reset	<i>Setting this bit causes the sensor to reset the automatic gain and exposure control logic. This is a self –resetting register bit and should always read "0". (This bit de-asserts internal active LOW reset signal for 15 clock cycles.)</i>	W
0x0D		Read Mode	
0-1	Row Bin	<i>0 = Normal operation 1 = Row bin 2. Two pixel rows are read per row output. Image size is effectively reduced by a factor of 2 vertically while data rate and pixel clock are not affected. Resulting frame rate is increased by 2. 2= Row bin 4. Four pixel rows are read per row output. Image size is effectively reduced by a factor of 4 vertically while data rate and pixel clock are not affected.</i>	W

		Resulting frame rate is increase by 4. 3 = Not valid	
2-3	Column Bin	0 = Normal operation. 1 = Column bin 2. When set, image size is reduced by a factor of 2 horizontally. Frame rate is not affected but data rate and pixel clock are reduced by one half that of the master clock. 2 = Column bin 4. When set, image size is reduced by a factor of 4 horizontally. Frame rate is not affected but data rate and pixel clock are reduced by one fourth that of master clock. 3 = Not valid	W
4	Row Flip	Read out rows from bottom to top (upside down). When set, row readout starts from row (Row Start + Window Height) and continues down to (Row Start + 1). When clear, readout starts a t row start and continues to (Row Start + Window Height – 1).	W
5	Column Flip	Read out columns from right to left (mirrored). When set, column readout starts from column (Col Start + Window Width) and continues down to (Row Start + 1). When clear, readout starts at Row Start and continues to (Row Start + Window Width – 1).	W
6	Show Dark Rows	When set, the programmed dark rows are output before the active window. Frame valid is thus asserted earlier than normal. This has no effect on integration time or frame rate. Whether the dark rows are shown in the image or not the definition frame start is before the dark rows are read out.	W
7	Show Dark Columns	When set, the programmed dark columns are output before the active pixels in a line. Line valid is thus asserted earlier than normal, and the horizontal blank time gets shorter by 18 pixel clocks.	W
0x0E		Monitor Mode	
0	Monitor Mode Enable	Setting this bit puts the sensor into a cycle of sleeping for five minutes and waking up to capture a programmable number of frames (register 0xC0). Clearing this bit (0) resumes normal operation	W
0x0F		Pixel Operation Mode	
6	High Dynamic Range	0 = Linear operation 1 = High dynamic range. Voltage and shutter width must be correctly set for saturation control to operate.	W
7	Enable Extended Exposure	When set, exposure is extended from half of frame time to full frame time (fro sequential mode only).	W
0x1B		LED_OUT Control	
0	Disable LED_OUT	Disable LED_OUT output. When cleared, the output pin LED_OUT is pulsed high when the sensor is undergoing exposure.	W
1	Invert LED_OUT	Invert polarity of LED_OUT output. When set, the output pin LED_OUT is pulsed low when the sensor is undergoing exposure.	W
0x1C		ADC Resolution Control	
0-1	ADC Mode	0 = Invalid 1 = Invalid 2 = 10-bit Linear. 3 = 12 to 10-bit companding.	W

0x2C		VREF_ADC control	
0-2	VREF_ADC Voltage Level	0 = VREF_ADC = 1.0V. 1 = VREF_ADC = 1.1V. 2 = VREF_ADC = 1.2V. 3 = VREF_ADC = 1.3V. 4 = VREF_ADC = 1.4V. (Effective ADC reference voltage is 1.0V) 5 = VREF_ADC = 1.5V. 6 = VREF_ADC = 1.6V. 7 = VREF_ADC = 2.1V.	W
0x31		V1 Control	
0-4	V1 voltage level	V_Step = bits (0-4) x 62.5mV + 0.5625V. Range: 0.5625 – 2.5V; Default: 2.375V. Usage: V_Step1 HiDy voltage.	W
0x32		V2 Control	
0-4	V2 voltage level	V_Step = bits (0-4) x 62.5mV + 0.5625V. Range: 0.5625 – 2.5V; Default: 2.0625V. Usage: V_Step2 HiDy voltage.	W
0x33		V3 Control	
0-4	V2 voltage level	V_Step = bits (0-4) x 62.5mV + 0.5625V. Range: 0.5625 – 2.5V; Default: 1.875V. Usage: V_Step3 HiDy voltage.	W
0x34		V4 Control	
0-4	V2 voltage level	V_Step = bits (0-4) x 62.5mV + 0.5625V. Range: 0.5625 – 2.5V; Default: 0.125V. Usage: V_Step HiDy parking voltage; also provides anti-blooming when V_Step is disabled.	W
0x35	Analog Gain		
0-6	Analog Gain	Analog gain = bits (0-6) x 0.0625. Range: 16(dec)-64(dec) for 1X-4X respectively. Column amplifier common gain. Note: No exception detection is installed; caution should be taken when programming.	W
0x36		Maximum Analog Gain	
0-6	Maximum Analog Gain	This register is used by the automatic gain control (AGC) as the upper threshold of gain. This ensures the new calibrated gain value does not exceed that which the sensor supports. Range: 16(dec)-64(dec) for 1X-4X respectively. Note: No exception detection is installed; caution should be taken when programming.	W
0x42		Frame Dark Average	
0-7	Frame Dark Average	The value read is the frame averaged black level that is used in the black level algorithm calculations.	R
0x46		Dark Average Thresholds	
0-7	Lower Threshold	Lower threshold for targeted black level in ADC LSBs.	W
8-15	Upper Threshold	Upper threshold for targeted black levels in ADC LSBs.	W
0x47		Black Level Calibration Control	
0	Manual Override	Manual override of black level correction 1 = Override automatic black level correction with programmed values (register 0x48). 0 = Normal operation	W
5-7	Frames to average over	Two to the power of this value decide how many frames to average over when the black level algorithm is in the	W

		<i>averaging mode. In this mode the running frame average is calculated from the following formula: Running frame average = old running frame average – (old running frame average)/2n + (new frame average) /2n.</i>	
0x48		Black Level Calibration Value	
0-7	<i>Black Level Calibration Value</i>	<i>Analog calibration offset: Negative numbers are represented with two's complement, which is shown in the following formula: Sign = bit 7 (0 is positive, 1 is negative). If positive offset value: Magnitude = bit 0-6 If negative offset value: Magnitude = not (bit 0-6) + 1. When read this register returns the user-programmed value when manual override is enable (register 0x47 bit 0); otherwise this register returns the result obtained from the calibration algorithm.</i>	W
0x4C		Black Level Calibration Value Step Size	
0-4	<i>Step Size of Calibration Value</i>	<i>This is the size calibration value may change (positively or negatively) from frame to frame. 1 calib LSB = ½ ADC LSB, assuming analog gain = 1</i>	W
0x70		Row Noise Correction Control 1	
0-3	<i>Number of Dark Pixels</i>	<i>The number of dark pixels used in the row-wise noise calculation. 0 = 2 pixels. 1 = 4 pixels. 2 = 6 pixels. 4 = 10 pixels. 8 = 18 pixels.</i>	W
5	<i>Enable Noise Correction</i>	<i>0 = Normal operation 1 = Enable row noise cancellation algorithm. When this bit is set, on a per row basis, the dark average is subtracted from each pixel in the row and then a constant (register 0x72) is added.</i>	W
11	<i>Use Black Level Average</i>	<i>1 = Use black level frame average from the dark rows in the row noise correction algorithm for low gains. This frame average was taken before the last adjustment of the offset DAC for that frame, so it might be slightly off. 0 = Use the average value of the dark columns read out in each row as dark average.</i>	W
0x72		Row Noise Constant	
0-7	<i>Row Noise Constant</i>	<i>Constant used in the row noise cancellation algorithm. It should be set to the dark level targeted by the black level algorithm plus the noise expected between the averaged values of dark columns. At default the constant is set to 42 LSB.</i>	W
0x073		Row Noise Correction Control 2	
0-9	<i>Dark Start Column Address</i>	<i>The starting column address for the dark columns to be used in the row-wise noise correction algorithm</i>	W
0x74		Pixel Clock, FRAME and LINE VALID Control	
0	<i>Invert Line Valid</i>	<i>Invert line valid. When set, LINE_VALID is reset to logic "0" when DOUT is valid.</i>	W
1	<i>Invert Frame Valid</i>	<i>Invert frame valid. When set, FRAME_VALID is reset to logic "0" when frame is valid.</i>	W
2	<i>X or Line Valid</i>	<i>1 = Line valid = "Continuous" Line Valid XOR Frame Valid 0 = Line Valid determined by bit 3. Ineffective if Continuous Line Valid is set.</i>	W

3	Continuous Line Valid	1 = "Continuous" Line Valid (continue producing line valid during vertical blank). 0 = Normal Line Valid (default, no line valid during vertical blank).	W
4	Invert Pixel Clock	Invert pixel clock. When set, LINE_VALID, FRAME_VALID and DOUT is set up to the rising edge of pixel clock, PIXCLK. When clear, they are set up to the falling edge of PIXCLK.	W
0x80 – 0x98		Tiled Digital Gain	
0-3	Tile Gain	Tile Digital Gain = Bits (0-3) x 0.25	W
4-7	Sample Weight	To indicate the weight of individual tile used in the automatic gain/exposure control algorithm.	W
0x99		Digital Tile Coordinate 1 – X-direction	
0-9	X0	The starting x-coordinate of digital tiles X0_*	W
0x9A		Digital Tile Coordinate 2 – X-direction	
0-9	X1	The starting x-coordinate of digital tiles X1_*	W
0x9B		Digital Tile Coordinate 3 – X-direction	
0-9	X2	The starting x-coordinate of digital tiles X2_*	W
0x9C		Digital Tile Coordinate 4 – X-direction	
0-9	X3	The starting x-coordinate of digital tiles X3_*	W
0x9D		Digital Tile Coordinate 5 – X-direction	
0-9	X4	The starting x-coordinate of digital tiles X4_*	W
0x9E		Digital Tile Coordinate 6 – X-direction	
0-9	X5	The starting x-coordinate of digital tiles X5_*	W
0x9F		Digital Tile Coordinate 1 – Y-direction	
0-8	Y0	The starting y-coordinate of digital tiles *_Y0.	W
0xA0		Digital Tile Coordinate 2 – Y-direction	
0-8	Y1	The starting y-coordinate of digital tiles *_Y1.	W
0xA1		Digital Tile Coordinate 3 – Y-direction	
0-8	Y2	The starting y-coordinate of digital tiles *_Y2.	W
0xA2		Digital Tile Coordinate 4 – Y-direction	
0-8	Y3	The starting y-coordinate of digital tiles *_Y3.	W
0xA3		Digital Tile Coordinate 5 – Y-direction	
0-8	Y4	The starting y-coordinate of digital tiles *_Y4.	W
0xA4		Digital Tile Coordinate 6 – Y-direction	
0-8	Y5	The starting y-coordinate of digital tiles *_Y5.	W
0xA5		AEC/AGC Desired Bin	
0-5	Desired Bin	User-defined "desired bin" that gives a measure of how bright the image is intended	W
0xA6		AEC Update Frequency	
0-3	Exp Skip Frame	The number of frames that the AEC must skip before updating the exposure register (register 0xBB)	W
0xA8		SEC Low Pass Filter	
0-1	Exp LPF	This value plays a role in determining the increment/decrement size of exposure value from frame to frame. If current bin does not = 0 (register 0xBC), When Exp LPF = 0: Actual new exposure = Calculated new exp. When Exp LPF = 1: If (calculated new exp – current exp) > (current exp/4), Actual new exposure = Calculated new exposure, otherwise Actual new exposure = Current exp +/- (calculated new exp / 2) When Exp LPF = 2: If (Calculated new exp – current exp) > (current exp/4),	W

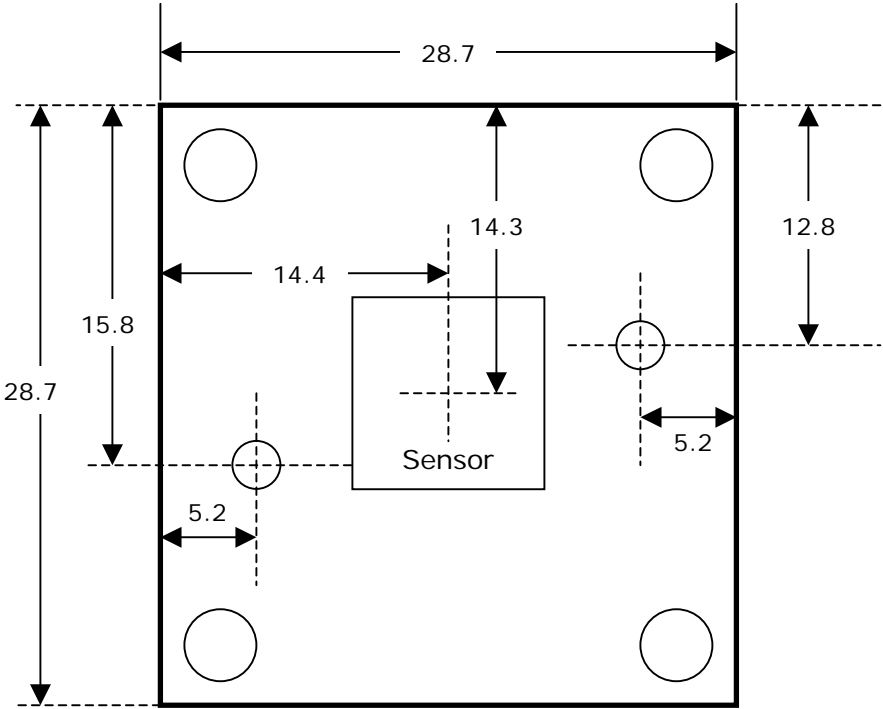
		Actual new exposure = Calculated new exposure, otherwise Actual new exposure = Current exp +/- (calculated new exp/4)	
0xA9		AGC Output Update Frequency	
0-1	Gain Skip Frame	The number of frames that the AGC must skip before updating the exposure register (register 0xBA).	W
0xAB		AGC Low Pass Filter	
0-1	Gain LPF	This value plays a role in determining the increment/decrement size of exposure value from frame to frame. If current bin does not = 0 (register 0xBC), When Gain LPF = 0: Actual new gain = Calculated new gain. When Gain LPF = 1: If (calculated new gain – current gain) > (current gain/4), Actual new gain = Calculated new gain, otherwise Actual new gain = Current gain +/- (calculated new gain / 2) When Gain LPF = 2: If (Calculated new gain – current gain) > (current gain/4), Actual new gain = Calculated new gain, otherwise Actual new gain = Current gain +/- (calculated new gain/4)	W
0xAF		AGC/AEC enable	
0	AEC Enable	0 = Disable Automatic Exposure Control 1 = Enable Automatic Exposure Control	W
1	AGC Enable	0 = Disable Automatic Gain Control 1 = Enable Automatic Gain Control	W
0xB0		AGC/AEC Pixel Count	
0-15	Pixel Count	The number of pixels used for the AEC/AGC histogram	W
0xB1		LVDS Master Control	
0	PLL Bypass	0 = Internal shift-CLK is driven by PLL. 1 = Internal shift-CLK is sourced from the LVDS_BYPASS_CLK.	W
1	LVDS Power-down	0 = Normal operation 1 = Power-down LVDS block	W
2	PLL Test Mode	0 = Normal operation 1 = The PLL output frequency is equal to the system clock frequency	W
3	LVDS Test Mode	0 = Normal operation 1 = The SER_DATAOUT_P drives a square wave.	W
0xB5		LVDS Internal Sync	
0	LVDS Internal Sync Enable	When set, the sensor generates a sync pattern (data with all zeros except start bit) on LVDS_SER_DATA_OUT.	W
0xB6		LVDS Payload Control	
0	Use 10-bit Pixel Enable	When set, all 10 bits contains pixel (with embedded controls) in stand-alone mode. If clear, payload is 8 bits of pixel with 2 bits of controls.	W
0xBA		ABC Gain Output	
0-6	AGC Gain	Status register to report the current gain value obtained from the AGC algorithm.	R
0xBB		AEC Exposure Output	
0-15	AEC Exposure	Status register to report the current exposure value obtained from the AEC algorithm	R
0xBC		AGC/AEC Current Bin	
0-5	Current Bin	Status register to report the current bin of the histogram	R

0xBD		Maximum total Shutter Width	
0-15	Maximum Total Shutter Width	This register is used by the automatic exposure control (AEC) as the upper threshold of exposure. This ensures the new calibrated integration value does not exceed that which the sensor supports.	W
0xBE		AGC/AEC Bin Difference Threshold	
0-7	Bin Difference Threshold	This register is used by the AEC only when exposure reaches its minimum value of 1. If the difference between desired bin (register 0xA5) and current bin (register 0xBC) is larger than the threshold, the exposure is increased.	W
0xBF		Field Vertical Blank	
0-8	Field Vertical Blank	The number of blank rows between odd and even fields. Note: For interlaced (both field) mode only. See register 0x07 bits 0-2	W
0xC0		Monitor Mode Capture Control	
0-7	Image Capture Number	The number of frames to be captured during the wake-up period when monitor mode is enabled.	W
0xC2		Analog Controls	
7	Anti-Eclipse Enable	Setting this bit turns on anti-eclipse circuitry.	W
11-13	V_rst_lim voltage Level	$V_rst_lim = bits (0-4) \times 50mV + 1.95V$ Range: 1.95 – 2.35V; Default: 2.15V Usage: For anti-eclipse reference voltage control	W
0xC3		NTSC Frame Valid Control	
0	Extend Frame Valid	When set, frame valid is extended for half-line in length at the odd field.	W
1	Replace FV/LV with Ped/Sync	When set, frame valid and line valid is replaced by ped and sync signals respectively.	W
0xC4	Control	NTSC Horizontal Blanking	
0-7	Front porch width	The front porch width in number of master clock cycles. NTSC standard is 1.5uSec +/-0.1uSec.	W
8-15	Sync Width	The pulse width in number of master clock cycles. NTSC standard is 4.7uSec +/-0.1uSec.	W
0xC5		NTSC Vertical Blanking Control	
0-7	Equalizing Pulse Width	The pulse width in number of master clock cycles. NTSC standard is 2.3uSec +/-0.1uSec.	W
8-15	Vertical Serration Width	The pulse width in number of master clock cycles. NTSC standard is 4.7uSec +/-0.1uSec.	W

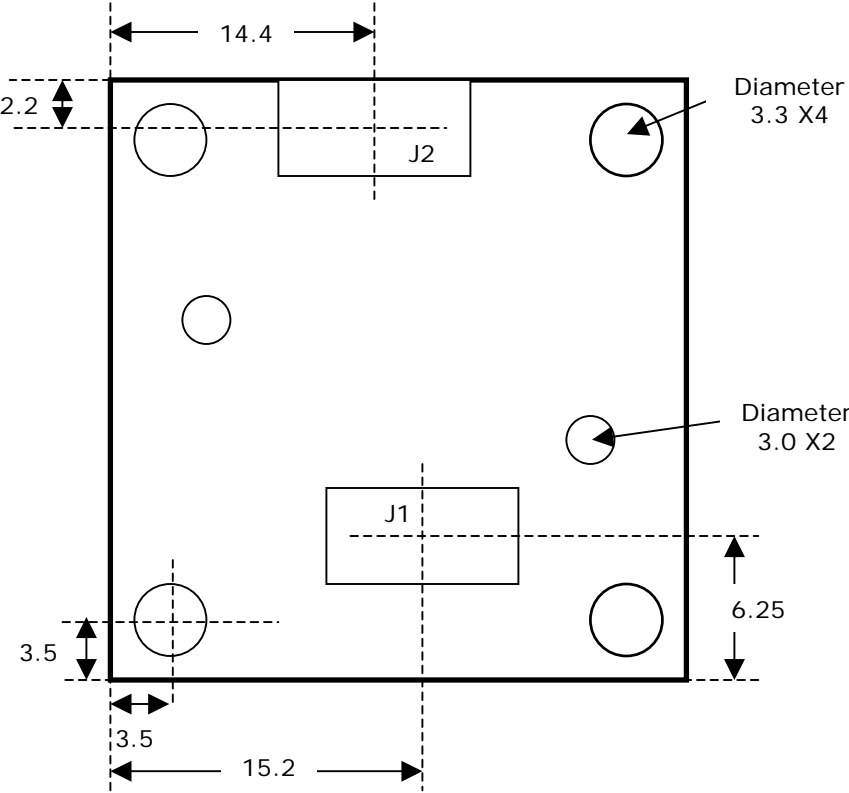
14.Mechanical Dimensions

(All dimensions in millimeters +/- 0.1 mm)

Front



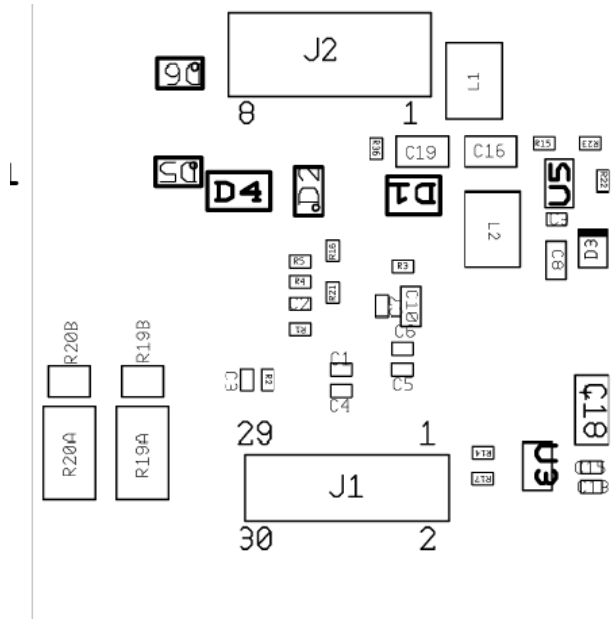
Back



15.Connection Diagram

J2 – 8 PIN JST (BM08B-SRSS-TB)

1 - 5-20V DC input
2 - GND
3 – Video out
4 – I2C Data
5 – I2C Clock
6 - GND
7 – SER DAT OUT + (LVDS)
8 – SER DAT OUT – (LVDS)



J1 – 30 PIN MOLEX – (53916-0301)

1 - GND	2 - GND
3 - DO0	4 - DO8
5 - DO1	6 - DO9
7 - DO2	8 - RESET
9 - DO3	10 - PIX CLK
11 - DO4	12 - STANDBY
13 - DO5	14 - SER DAT OUT + (LVDS)
15 - DO6	16 - SER DAT OUT – (LVDS)
17 - DO7	18 - LINE
19 - SYSCLOCK	20 - FRAME
21 - GND	22 - GND
23 - LED OUT	24 - N/C
25 - ERROR	24 - N/C
27 - I2C Data	28 - I2C Clock
29 - Video Out	30 - 5-20V DC input
30 Pin Molex mating connector 52991-0308	

16.Contact

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<http://www.videologyinc.com/>

Please note that data in this application note is subject to change without notification!

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Doc # APN 24B752xA	Issue Date: 11/21/2008
Revision: C	Page 22 of 22